WHAT IS CLAIMED IS:

1. A p-channel depletion mode floating gate transistor, comprising:

a first source/drain region and a second source/drain region separated by a depletion mode p-type channel region in an n-type substrate;

a floating gate opposing the p-type channel region and separated therefrom by a gate oxide;

a control gate opposing the floating gate; and

wherein the control gate is separated from the floating gate by an asymmetrical low tunnel barrier intergate insulator.

2. The p-channel depletion mode floating gate transistor of claim 1, wherein the asymmetrical low tunnel barrier intergate insulator includes aluminum oxide (Al_2O_3), wherein the aluminum oxide has a number of small compositional ranges such that gradients which produce different barrier heights at an interface with the floating gate and control gate.

3. The p-channel depletion mode floating gate transistor of claim 1, wherein the asymmetrical low tunnel barrier intergate insulator includes an asymmetrical transition metal oxide.

4. The p-channel depletion mode floating gate transistor of claim 3, wherein the asymmetrical transition metal oxide is selected from the group consisting of Ta_2O_5, TiO_2, ZrO_2, and Nb_2O_5.

5. The p-channel depletion mode floating gate transistor of claim 1, wherein the asymmetrical low tunnel barrier intergate insulator includes an asymmetrical Perovskite oxide tunnel barrier.

6. The p-channel depletion mode floating gate transistor of claim 5, wherein the asymmetrical Perovskite oxide tunnel barrier is selected from the group consisting of $SrBi_2Ta_2O_3$, $SrTiO_3$, $PbTiO_3$, and $PbZrO_3$.

7. The p-channel depletion mode floating gate transistor of claim 1, wherein the floating gate includes a polysilicon floating gate having a metal layer formed thereon in contact with the asymmetrical low tunnel barrier intergate insulator.

8. The p-channel depletion mode floating gate transistor of claim 7, wherein the control gate includes a polysilicon control gate having a metal layer formed thereon in contact with the low tunnel barrier intergate insulator, wherein the metal layer includes a metal layer that has a different work function than the metal layer formed on the floating gate.

9. A vertical, p-channel depletion mode non volatile memory cell, comprising:

a first source/drain region formed on a substrate;

a body region including a p-type depletion mode channel region formed on the first source/drain region;

a second source/drain region formed on the body region;

a floating gate opposing the channel region and separated therefrom by a gate oxide;

a control gate opposing the floating gate; and

wherein the control gate is separated from the floating gate by an asymmetrical low tunnel barrier intergate insulator having a number of small compositional ranges such that gradients can be formed which produce different barrier heights at an interface with the floating gate and control gate.

10. The vertical, p-channel depletion mode non volatile memory cell of claim 9, wherein the asymmetrical low tunnel barrier intergate insulator includes an insulator selected from the group consisting of Al_2O_3, Ta_2O_5, TiO_2, ZrO_2, Nb_2O_5, $SrBi_2Ta_2O_3$, $SrTiO_3$, $PbTiO_3$, and $PbZrO_3$.

11. The vertical, p-channel depletion mode non volatile memory cell of claim 9, wherein the floating gate includes a polysilicon floating gate having a metal layer formed thereon in contact with the asymmetrical low tunnel barrier intergate insulator.

12. The vertical, p-channel depletion mode non volatile memory cell of claim 11, wherein the control gate includes a polysilicon control gate having a metal layer formed thereon in contact with the low tunnel barrier intergate insulator, wherein the metal layer includes a metal layer that has a different work function than the metal layer formed on the floating gate.

13. The vertical, p-channel depletion mode non volatile memory cell of claim 9, wherein the floating gate includes a vertical floating gate formed alongside of the body region.

14. The vertical, p-channel depletion mode non volatile memory cell of claim 13, wherein the control gate includes a vertical control gate formed alongside of the vertical floating gate.

15. The vertical, p-channel depletion mode non volatile memory cell of claim 9, wherein the floating gate includes a horizontally oriented floating gate formed alongside of the body region.

16. The vertical, p-channel depletion mode non volatile memory cell of claim 15, wherein the control gate includes a horizontally oriented control gate formed above the horizontally oriented floating gate.

17. A non-volatile memory cell, comprising:

a first source/drain region and a second source/drain region separated by a p-type channel region in an n-type substrate;

a polysilicon floating gate opposing the channel region and separated therefrom by a gate oxide;

a first metal layer formed on the polysilicon floating gate;

a metal oxide intergate insulator formed on the metal layer, wherein the metal oxide intergate insulator includes an asymmetrical metal oxide having a number of small compositional ranges such that gradients can be formed in an applied electric field which produce different barrier heights at an interface with the floating gate and control gate;

a second metal layer formed on the metal oxide intergate insulator, wherein the second metal layer has a different work function from the first metal layer; and

a polysilicon control gate formed on the second metal layer.

18. The non-volatile memory cell of claim 17, wherein first metal layer includes a parent metal for the asymmetrical metal oxide and the second metal layer includes a metal layer having a work function in the range of 2.7 eV to 5.8 eV.

19. The non-volatile memory cell of claim 17, wherein the second metal layer is platinum (Pt) and the metal oxide intergate insulator is selected from the group consisting of TiO_2, $SrTiO_3$, $PbTiO_3$, and $PbZrO_3$.

20. The non-volatile memory cell of claim 17, wherein the second metal layer is aluminum and the metal oxide intergate insulator is selected from the group consisting of Ta_2O_5, ZrO_2, $SrBi_2Ta_2O_3$, $SrTiO_3$, $PbTiO_3$, and $PbZrO_3$.

21. The non-volatile memory cell of claim 17, wherein the metal oxide intergate insulator is selected from the group consisting of Al_2O_3, Ta_2O_5, TiO_2, ZrO_2, Nb_2O_5, $SrBi_2Ta_2O_3$, $SrTiO_3$, $PbTiO_3$, and $PbZrO_3$.

22. The non-volatile memory cell of claim 17, wherein the floating gate transistor includes a vertical floating gate transistor.

23. A flash memory array, comprising:

a number of p-channel depletion mode, non-volatile memory cells, wherein each non-volatile memory cell includes:

a first source/drain region and a second source/drain region separated by a depletion mode p-channel region;

a floating gate opposing the p-channel region and separated therefrom by a gate oxide;

a control gate opposing the floating gate; and

wherein the control gate is separated from the floating gate by an asymmetrical low tunnel barrier intergate insulator having a number of small compositional ranges such that gradients can be formed which produce different barrier heights at an interface with the floating gate and control gate;

a number of sourcelines coupled to the first source/drain regions along a first selected direction in the flash memory array;

a number of control gate lines coupled to the control gates along a second

selected direction in the flash memory array; and

a number of bitlines coupled to the second source/drain regions along a third selected direction in the flash memory array.

24. The flash memory array of claim 23, wherein the asymmetrical low tunnel barrier intergate insulator includes a metal oxide insulator selected from the group consisting of Al_2O_3, Ta_2O_5, TiO_2, ZrO_2, Nb_2O_5, $SrBi_2Ta_2O_3$, $SrTiO_3$, $PbTiO_3$, and $PbZrO_3$.

25. The flash memory array of claim 23, wherein the floating gate includes a polysilicon floating gate having a metal layer formed thereon in contact with the asymmetrical low tunnel barrier intergate insulator.

26. The flash memory array of claim 25, wherein the control gate includes a polysilicon control gate having a metal layer formed thereon in contact with the asymmetrical low tunnel barrier intergate insulator, wherein the metal layer formed on the polysilicon control gate includes a metal layer that has a different work function than the metal layer formed on the floating gate.

27. The flash memory array of claim 26, wherein metal layer formed on the floating gate includes a parent metal for the asymmetrical low tunnel barrier intergate insulator and the metal layer formed on the control gate includes a metal layer having a work function in the range of 2.7 eV to 5.8 eV.

28. The flash memory array of claim 23, wherein the second selected direction and the third selected direction are parallel to one another and orthogonal to the first selected direction, and wherein the number of control gate lines serve as address lines.

29. The flash memory array of claim 23, wherein the first selected direction and the third selected direction are parallel to one another and orthogonal to the second selected direction, and wherein the number of control gate lines serve as address lines.

30. The flash memory array of claim 23, wherein the first selected direction and the second selected direction are parallel to one another and orthogonal to the third selected direction, and wherein the number of bitlines serve as address lines.

31. An array of flash memory cells, comprising:

a number of pillars extending outwardly from a substrate, wherein each pillar includes a first source/drain region, a body region having a p-type channel, and a second source/drain region;

a number of floating gates opposing the body regions in the number of pillars and separated therefrom by a gate oxide;

a number of control gates opposing the floating gates;

a number of buried sourcelines disposed below the number of pillars and coupled to the first source/drain regions along a first selected direction in the array of memory cells;

a number of control gate lines formed integrally with the number of control gates along a second selected direction in the array of flash memory cells, wherein the number of control gates are separated from the floating gates by a low tunnel barrier intergate insulator having a number of small compositional ranges such that gradients can be formed by an applied electric field which produce different barrier heights at an interface with the floating gate and control gate; and

a number of bitlines coupled to the second source/drain regions along a third selected direction in the array of flash cells.

32. The array of flash memory cells of claim 31, wherein the low tunnel barrier intergate insulator includes a metal oxide insulator selected from the group consisting of Al_2O_3, Ta_2O_5, TiO_2, ZrO_2, Nb_2O_5, $SrBi_2Ta_2O_3$, $SrTiO_3$, $PbTiO_3$, and $PbZrO_3$.

33. The array of flash memory cells of claim 31, wherein each floating gate includes a polysilicon floating gate having a metal layer formed thereon in contact with the asymmetrical low tunnel barrier intergate insulator.

34. The array of flash memory cells of claim 33, wherein each control gate includes a polysilicon control gate having a metal layer formed thereon in contact with the low tunnel barrier intergate insulator, wherein the metal layer formed on the polysilicon control gate includes a metal layer that has a different work function than the metal layer formed on the floating gate.

35. The array of flash memory cells of claim 34, wherein metal layer formed on the floating gate includes a parent metal for the asymmetrical low tunnel barrier intergate insulator and the metal layer formed on the control gate includes a metal layer having a work function in the range of 2.7 eV to 5.8 eV.

36. The array of flash memory cells of claim 31, wherein each floating gate is a vertical floating gate formed in a trench below a top surface of each pillar such that each trench houses a pair of floating gates opposing the body regions in adjacent pillars on opposing sides of the trench.

37. The array of flash memory cells of claim 31, wherein the number of control gate lines are formed in the trench below the top surface of the pillar and between the pair of floating gates, wherein each pair of floating gates shares a single control gate line, and wherein each floating gate includes a vertically oriented floating gate having a vertical length of less than 100 nanometers.

38. The array of flash memory cells of claim 31, wherein the number of control gate lines are formed in the trench below the top surface of the pillar and between the pair of floating gates such that each trench houses a pair of control gate lines each addressing the floating gates one on opposing sides of the trench respectively, and wherein the pair of control gate lines are separated by an insulator layer.

39. The array of flash memory cells of claim 31, wherein the number of control gate lines are disposed vertically above the floating gates, and wherein each pair of floating gates shares a single control gate line.

40. The array of flash memory cells of claim 31, wherein the number of control gate lines are disposed vertically above the floating gates, and wherein each one of the pair of floating gates is addressed by an independent one of the plurality of control gate lines.

41. The array of flash memory cells of claim 31, wherein each floating gate is a horizontally oriented floating gate formed in a trench below a top surface of each pillar such that each trench houses a floating gate opposing the body regions in adjacent pillars on opposing sides of the trench, and wherein each horizontally oriented floating gate has a vertical length of less than 100 nanometers opposing the body region of the pillars.

42. The array of flash memory cells of claim 41, wherein the plurality of control gate lines are disposed vertically above the floating gates.

43. A programmable logic array, comprising:

a plurality of input lines for receiving an input signal;

a plurality of output lines; and

one or more arrays having a first logic plane and a second logic plane connected between the input lines and the output lines, wherein the first logic plane and the second logic plane comprise a plurality of logic cells arranged in rows and columns for providing a sum-of-products term on the output lines responsive to a received input signal, wherein each logic cell includes a vertical p-type non-volatile memory cell including:

a first source/drain region formed on an n-type substrate;

a body region including a p-type channel region formed on the first source/drain region;

a second source/drain region formed on the body region;

a floating gate opposing the p-type channel region and separated therefrom by a gate oxide;

a control gate opposing the floating gate; and

wherein the control gate is separated from the floating gate by a low tunnel barrier intergate insulator having a number of small compositional ranges such that gradients can be formed by an applied electric field which produce different barrier heights at an interface with the floating gate and control gate.

44. An electronic system, comprising:

a processor; and

a memory device coupled to the processor, wherein the memory device and/or processor includes an array of p-channel depletion mode flash memory cells, comprising:

a number of pillars extending outwardly from a substrate, wherein each pillar includes a first source/drain region, a body region having a p-type depletion mode channel region, and a second source/drain region;

a number of floating gates opposing the body regions in the number of pillars and separated therefrom by a gate oxide;

a number of control gates opposing the floating gates;

a number of buried sourcelines disposed below the number of pillars and coupled to the first source/drain regions along a first selected direction in the array of memory cells;

a number of control gate lines formed integrally with the number of control gates along a second selected direction in the array of flash memory cells, wherein the number of control gates are separated from the floating gates by a low tunnel barrier intergate insulator having a number of small compositional ranges such that gradients can be formed by an applied electric field which produce different barrier heights at an interface with the floating gate and control gate; and

a number of bitlines coupled to the second source/drain regions along a third selected direction in the array of flash cells.

45. The electronic system of claim 44, wherein the asymmetrical low tunnel barrier intergate insulator includes a metal oxide insulator selected from the group consisting of Al_2O_3, Ta_2O_5, TiO_2, ZrO_2, Nb_2O_5, $SrBi_2Ta_2O_3$, $SrTiO_3$, $PbTiO_3$, and $PbZrO_3$.

46. The electronic system of claim 44, wherein each floating gate includes a polysilicon floating gate having a metal layer formed thereon in contact with the low tunnel barrier intergate insulator.

47. The electronic system of claim 44, wherein each control gate includes a polysilicon control gate having a metal layer formed thereon in contact with the low tunnel barrier intergate insulator, wherein the metal layer formed on the polysilicon control gate includes a metal layer that has a different work function than the metal layer formed on the floating gate.

48. The electronic system of claim 47, wherein metal layer formed on the floating gate includes a parent metal for the asymmetrical low tunnel barrier intergate insulator and the metal layer formed on the control gate includes a metal layer having a work function in the range of 2.7 eV to 5.8 eV.

49. The electronic system of claim 44, wherein each floating gate is a vertical floating gate formed in a trench below a top surface of each pillar such that each trench houses a pair of floating gates opposing the body regions in adjacent pillars on opposing sides of the trench.

50. The electronic system of claim 44, wherein the plurality of control gate lines are formed in the trench below the top surface of the pillar and between the pair of floating gates, wherein each pair of floating gates shares a single control gate line, and wherein each floating gate includes a vertically oriented floating gate having a vertical length of less than 100 nanometers.

51. The electronic system of claim 44, wherein the plurality of control gate lines are formed in the trench below the top surface of the pillar and between the pair of floating gates such that each trench houses a pair of control gate lines each addressing the floating gates one on opposing sides of the trench respectively, and wherein the pair of control gate lines are separated by an insulator layer.

52. The electronic system of claim 44, wherein the plurality of control gate lines are disposed vertically above the floating gates, and wherein each pair of floating gates shares a single control gate line.

53. The electronic system of claim 44, wherein the plurality of control gate lines are disposed vertically above the floating gates, and wherein each one of the pair of floating gates is addressed by an independent one of the plurality of control lines.

54. The electronic system of claim 44, wherein each floating gate is a horizontally oriented floating gate formed in a trench below a top surface of each pillar such that each trench houses a floating gate opposing the body regions in adjacent pillars on opposing sides of the trench, and wherein each horizontally oriented floating gate has a vertical length of less than 100 nanometers opposing the body region of the pillars.

55. The electronic system of claim 54, wherein the plurality of control gate lines are disposed vertically above the floating gates.

56. A method of forming a floating gate transistor, comprising:

forming a first source/drain region and a second source/drain region separated by a p-type channel region in an n-type substrate;

forming a floating gate opposing the p-type channel region and separated therefrom by a gate oxide;

forming a control gate opposing the floating gate; and

forming an asymmetrical low tunnel barrier intergate insulator to separate the control gate from the floating gate, wherein forming the low tunnel barrier intergate insulator includes a forming low tunnel barrier intergate insulator having a number of small compositional ranges such that gradients can be formed by an applied electric field which produce different barrier heights at an interface with the floating gate and control gate.

57. The method of claim 56, wherein forming the asymmetrical low tunnel barrier intergate insulator includes forming a metal oxide insulator selected from the group consisting of Al_2O_3, Ta_2O_5, TiO_2, ZrO_2, Nb_2O_5, $SrBi_2Ta_2O_3$, $SrTiO_3$, $PbTiO_3$, and $PbZrO_3$.

58. The method of claim 56, wherein forming the floating gate includes forming a polysilicon floating gate having a metal layer formed thereon in contact with the asymmetrical low tunnel barrier intergate insulator.

59. The method of claim 58, wherein forming the control gate includes a forming a polysilicon control gate having a metal layer formed thereon in contact with the low tunnel barrier intergate insulator, wherein the metal layer formed on the polysilicon control gate includes a metal layer that has a different work function than the metal layer formed on the floating gate.

60. The method of claim 59, wherein forming the metal layer on the floating gate includes a parent metal for the asymmetrical low tunnel barrier intergate insulator and the metal layer formed on the control gate includes a metal layer having a work function in the range of 2.7 eV to 5.8 eV.

61. A method for forming an array of flash memory cells, comprising:

forming a number of pillars extending outwardly from a substrate, wherein each pillar includes a first source/drain region, a body region having a p-type channel region, and a second source/drain region;

forming a number of floating gates opposing the body regions in the number of pillars and separated therefrom by a gate oxide;

forming a number of control gates opposing the floating gates;

forming a number of buried sourcelines disposed below the number of pillars and coupled to the first source/drain regions along a first selected direction in the array of memory cells;

forming a number of control gate lines formed integrally with the number of control gates along a second selected direction in the array of flash memory cells, wherein the number of control gates lines are separated from the floating gates by an asymmetrical low tunnel barrier intergate insulator, wherein forming the asymmetrical low tunnel barrier intergate insulator includes a forming low tunnel barrier intergate insulator having a number of small compositional ranges such that

gradients can be formed by an applied electric field which produce different barrier heights at an interface with the floating gate and control gate; and

forming a number of bitlines coupled to the second source/drain regions along a third selected direction in the array of flash cells.

62. The method of claim 61, wherein forming the asymmetrical low tunnel barrier intergate insulator includes forming a metal oxide insulator selected from the group consisting of Al_2O_3, Ta_2O_5, TiO_2, ZrO_2, Nb_2O_5, $SrBi_2Ta_2O_3$, $SrTiO_3$, $PbTiO_3$, and $PbZrO_3$.

63. The method of claim 61, wherein forming each floating gate includes forming a polysilicon floating gate having a metal layer formed thereon in contact with the low tunnel barrier intergate insulator.

64. The method of claim 63, wherein forming each control gate includes forming a polysilicon control gate having a metal layer formed thereon in contact with the low tunnel barrier intergate insulator, wherein the metal layer formed on the polysilicon control gate includes a metal layer that has a different work function than the metal layer formed on the floating gate.

65. The method of claim 64, wherein forming the metal layer on the floating gate includes a parent metal for the asymmetrical low tunnel barrier intergate insulator and the metal layer formed on the control gate includes a metal layer having a work function in the range of 2.7 eV to 5.8 eV.

66. The method of claim 61, wherein forming each floating gate includes forming a vertical floating gate in a trench below a top surface of each pillar such that each trench houses a pair of floating gates opposing the body regions in adjacent pillars on opposing sides of the trench.

67. The method of claim 61, wherein forming the plurality of control gate lines includes forming each control gate line in the trench below the top surface of the pillar and between the pair of floating gates, wherein each pair of floating gates shares a single control gate line, and wherein each floating gate includes a vertically oriented floating gate having a vertical length of less than 100 nanometers.

68. The method of claim 61, wherein forming the plurality of control gate lines includes forming a pair of control gate lines in each trench below the top surface of the pillar and between the pair of floating gates such that each control gate line addresses a floating gate on opposing sides of the trench respectively, and wherein the pair of control gate lines are separated by an insulator layer.

69. The method of claim 61, wherein forming the plurality of control gate lines includes forming the control gate lines such that the control gate lines are disposed vertically above the floating gates such that each pair of floating gates shares a single control gate line.

70. The method of claim 61, wherein forming the plurality of control gate lines includes forming the control gate lines such that the control gate lines are disposed vertically above the floating gates, and forming the plurality of control lines such that each one of the pair of floating gates is addressed by an independent one of the plurality of control lines.

71. The method of claim 61, wherein forming each floating gate includes forming a horizontally oriented floating gate in a trench below a top surface of each pillar such that each trench houses a floating gate opposing the body regions in adjacent pillars on opposite sides of the trench, and wherein each horizontally oriented floating gate has a vertical length of less than 100 nanometers opposing the body region of the pillars.

72. The method of claim 71, wherein the forming the plurality of control gate lines includes forming the control gate lines such that the control gate lines are disposed vertically above the floating gates.

73. A method for operating a p-type non-volatile memory cell, comprising:

writing to a floating gate of the p-type non-volatile memory cell using channel hot electron injection, wherein the p-type non–volatile memory cell includes:

a first source/drain region and a second source/drain region separated by a p-type channel region in an n-type substrate;

a floating gate opposing the p-type channel region and separated therefrom by a gate oxide;

a control gate opposing the floating gate; and

wherein the control gate is separated from the floating gate by an asymmetrical low tunnel barrier intergate insulator having a number of small compositional ranges such that gradients can be formed by an applied electric field which produce different barrier heights at an interface with the floating gate and control gate;

erasing charge from the floating gate by tunneling electrons off of the floating gate and onto the control gate through the asymmetrical low tunnel barrier insulator.

74. The method of claim 73, wherein erasing charge from the floating gate by tunneling electrons off of the floating gate and onto the control gate further through the asymmetrical low tunnel barrier insulator includes:

providing a negative voltage to the substrate; and

providing a large positive voltage to the control gate.

75. The method of claim 73, wherein the method further includes writing to the floating gate by tunneling electrons from the control gate to the floating gate through the asymmetrical low tunnel barrier insulator.

76. The method of claim 75, wherein writing to the floating gate by tunneling electrons from the control gate to the floating gate through the asymmetrical low tunnel barrier insulator further includes:

applying a positive voltage to the substrate; and

applying a large negative voltage to the control gate.

77. The method of claim 73, wherein tunneling electrons from the floating gate to the control gate through the asymmetrical low tunnel barrier insulator includes tunneling electrons from the floating gate to the control gate through an asymmetrical low tunnel barrier insulator selected from the group consisting of Al_2O_3, Ta_2O_5, TiO_2, ZrO_2, Nb_2O_5, $SrBi_2Ta_2O_3$, $SrTiO_3$, $PbTiO_3$, and $PbZrO_3$.

78. The method of claim 72, wherein tunneling electrons from the floating gate to the control gate through the asymmetrical low tunnel barrier insulator includes tunneling electrons through the asymmetrical low tunnel barrier insulator having a barrier energy of approximately 2.0 eV.

79. The method of claim 72, wherein tunneling electrons from the floating gate to the control gate through the asymmetrical low tunnel barrier insulator includes tunneling electrons from a metal layer formed on the floating gate in contact with the low tunnel barrier intergate insulator to a metal layer formed on the control gate and also in contact with the low tunnel barrier intergate insulator.

80. A method for operating an array of p-channel flash memory cells, comprising:

writing to one or more floating gates for a number of p-type non-volatile memory cells in the array of p-channel flash memory cells using channel hot electron injection, the array of flash memory cells includes:

a number of pillars extending outwardly from a substrate, wherein each pillar includes a first source/drain region, a body region having a p-type channel, and a second source/drain region;

a number of floating gates opposing the body regions in the number of pillars and separated therefrom by a gate oxide;

a number of control gates opposing the floating gates;

a number of buried sourcelines disposed below the number of pillars and coupled to the first source/drain regions along a first selected direction in the array of memory cells;

a number of control gate lines formed integrally with the number of control gates along a second selected direction in the array of flash memory cells, wherein the number of control gates lines

are separated from the floating gates by an asymmetrical low tunnel barrier intergate insulator having a number of small compositional ranges such that gradients can be formed by an applied electric field which produce different barrier heights at an interface with the floating gate and control gate; and

a number of bitlines coupled to the second source/drain regions along a third selected direction in the array of flash cells; and

erasing charge from the one or more floating gates by tunneling electrons off of the one or more floating gates and onto the number of control gates through the asymmetrical low tunnel barrier insulator.

81. The method of claim 80, wherein erasing charge from the one or more floating gates by tunneling electrons off of the floating gate and onto the number of control gate through the asymmetrical low tunnel barrier insulator further includes:

providing a negative voltage to a substrate of one or more p-type non-volatile memory cells; and

providing a large positive voltage to the control gate for the one or more p-type non-volatile memory cells.

82. The method of claim 81, wherein the method further includes erasing an entire row of non-volatile memory cells by providing a negative voltage to all of the substrates along an entire row of p-type non-volatile memory cells and providing a large positive voltage to all of the control gates along the entire row of non-volatile memory cells.

83. The method of claim 81, wherein the method further includes erasing an entire block of non-volatile memory cells by providing a negative voltage to all of the substrates along multiple rows of non-volatile memory cells and providing a large positive voltage to all of the control gates along the multiple rows of non-volatile memory cells.